REMARKS

Claims 15, 16, 23-30 and 32-35 have been rejected under 35 U.S.C. 102(b), as being anticipated by Petersen (U.S. Patent No. 5,517,627.)

Claim 15 recites "incrementing a read pointer of the memory device each time a data word is read from the memory device" and "adjusting the read pointer at the end of the fly-by read operation".

The Examiner indicates that Petersen teaches both of these elements of Claim 15 at column 13, lines 12-13 and lines 47-50. The Examiner further indicates that "the queue count value is the read pointer."

However, column 13, lines 12-13 of Petersen recites "After transitioning from block 140, the queue count value is reset in block 141". This section merely indicates that the queue count value is reset at the start of the device.

Column 13, lines 47-50 of Petersen recites "In block 151, the next queue count value is set to the total read data value minus 1. If the total read data value is not greater than or equal to 4, the next queue count value is set to the total read data value in block 151." This section of Petersen indicates that the next queue count value is handled in different manners, depending on a total read data value. Thus, Petersen fails to teach incrementing the queue count value each time a data word is read from the memory device. Consequently, Petersen fails to teach "incrementing a read pointer of the memory device each time a data word is read from the memory device" as recited by Claim 15.

In addition, Petersen clearly teaches that for each assertion of the HOST READ ENABLE signal (Petersen, Fig. 13, block 142), there is only one adjustment to the queue count

PAGE 15/22 * RCVD AT 3/29/2004 4:37:57 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:9253718187 * DURATION (mm-ss):05-38

value (Petersen, Fig. 13, block 151 or block 152). Thus, Petersen clearly fails to teach both incrementing the queue count value each time a data word is read from the memory device AND adjusting the queue count value at the end of the operation. Thus, Petersen fails to teach both "incrementing a read pointer of the memory device each time a data word is read from the memory device" and "adjusting the read pointer at the end of the fly-by read operation" as recited by Claim 15.

For these reasons, Claim 15 is not anticipated by Petersen. Claims 16 and 23, which depend from Claim 15, are not anticipated by Petersen for at least the same reasons as Claim 15.

In addition, Claim 16 recites "providing byte enable signals on the system bus using a direct memory access (DMA) controller".

The Examiner indicates that Petersen teaches the use of a DMA controller to provide byte enable signals at column 12, lines 17-37. However, this section of Petersen does not mention a DMA controller. In addition, Petersen explicitly states "the BYTE ENABLE signals ... are generated from the host". (Petersen, Col. 13, lines 58-60.) Because Petersen teaches that the host generates the byte enable signals, Petersen fails to teach the use of a DMA controller to provide byte enable signals. For this additional reason, Claim 16 is not anticipated by Petersen.

Claim 24 recites "reading a first data word from the memory device, ... such that the first data word includes a first set of one or more bytes to be included in the fly-by write operation, and a second set of one or more bytes to be excluded from the fly-by write operation" and "transmitting an invalid data word on the system bus to a slave device,

PAGE 16/22 * RCVD AT 3/29/2004 4:37:57 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:9253718187 * DURATION (mm-ss):05-38

wherein the invalid data word includes the second set of one or more bytes of the first data word".

The Examiner indicates that Petersen teaches all the steps of Claim 24 at Col. 4, lines 43-67, Col. 5, lines 17-25 and Table 1.

Petersen explicitly teaches that "Each [input] segment lane L1(0) through L1(N) is used to transfer segments of data from the host data bus to shifter 1" of the write data aligner. (Emphasis added.) (Petersen, Col. 4, lines 1-3.) TABLE 1 of Petersen indicates that at least one valid byte is transmitted on the host bus L1(3), L1(2), L1(1) and L1(0) during each write cycle of the write data aligner. Because Petersen always includes at least one valid byte on the host bus, Petersen fails to teach transmitting an invalid word on the host bus. Note the undesirable result in TABLE 1 of Petersen, wherein it takes 11 write cycles to transfer 24 bytes (6 words). Also note that if Petersen did not have at least one valid byte on the host bus, there would be no reason to implement a write cycle.

Because Petersen fails to teach transmitting an invalid word on the host bus, Petersen fails to teach "transmitting an invalid data word on the system bus" as recited by Claim 24.

For these reasons, Claim 24 is not anticipated by Petersen. Claims 25-30 and 32, which depend from Claim 24, are not anticipated by Petersen for at least the same reasons as Claim 24.

In addition, Claim 27 recites "reading a second data word from the memory device", "combining the first set of one or more bytes of the first data word with a first set of one or more bytes of the second data word to create a first

PAGE 17/22 * RCVD AT 3/29/2004 4:37:57 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:9253718187 * DURATION (mm-ss):05-38

fly-by write data word", and "transmitting the first fly-by write data word on the system bus to the slave device".

Petersen fails to teach combining a first set of bytes from a first data word with a second set of bytes of a second data word to create a write data word, and then transmitting the write data word on the host bus L1(0), L1(1), L1(2) and L1(3). In fact, Petersen clearly teaches that bytes of different words are not to be combined. See, for example, the fifth through eighth write cycles, wherein bytes 12, 13, 14 and 15 are sent separately on the host data bus, rather than being combined. For this additional reason, Claim 27 is not anticipated by Petersen.

Claim 33 recites "reading a first data word from a first memory device; preloading the first data word into a read aligner; and then reading a second data word from the first memory device; applying the second data word to the read aligner; applying a first alignment signal to the read aligner; creating a first fly-by read word by routing a first portion of the first data word and a first portion of the second data word through the read aligner in response to the first alignment signal; and transmitting the first fly-by read word on a system bus to a write aligner." (Emphasis added.)

The Examiner indicates that the elements of Claim 33 are taught by Petersen at Col. 7, line 45 to Col. 9, line 46. The cited section of Petersen discloses the read data aligner of Fig. 2. This while this read data aligner may transmit a data word on host data bus segment lanes O2(0) to O2(3) (Petersen, Col. 8, lines 1-9), Petersen fails to teach that this data word is transmitted to "a write aligner" as recited by Claim 33. In fact, Petersen teaches that both the write data aligner (Fig. 1) and the read data aligner

PAGE 18/22 * RCVD AT 3/29/2004 4:37:57 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:9253718187 * DURATION (mm-ss):05-38

(Fig. 2) are located in the same peripheral device 15 (Fig. 7, 8, 9 12). Thus, data transmitted from the read data aligner would not be transmitted to the write data aligner, but rather to the host data bus.

For these reasons, Claim 33 is not anticipated by Petersen. Claims 34 and 35, which depend from Claim 33, are not anticipated by Petersen for at least the same reasons as Claim 33.

Claims 1-14 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Petersen in view of Chauvel et al. (U.S. Patent No. 6,412,048), hereinafter "Chauvel".

Claim 1 recites "a memory control device coupled to the system bus and the DMA controller, the memory control device including a memory controller, a memory read aligner, a memory write aligner and a memory slave interface".

The Examiner correctly indicates that Petersen does not teach a memory control device as recited by Claim 1. The Examiner indicates that Chauvel teaches a memory control device as recited by Claim 1. More specifically, the Examiner indicates that traffic controller 18, as described by Col. 9, lines 29-59 of Chauvel corresponds with a memory control device as recited by Claim 1.

However, traffic controller 18 does not include "a memory controller, a memory read aligner, a memory write aligner, and a memory slave interface" as recited by Claim 1. If the Examiner believes that traffic controller 18 of Chauvel teaches these elements of Claim 1, it is the Examiner's burden to specifically point out where these elements are shown in Chauvel. The cited portion of Chauvel merely discusses the manner in which access commands are generated by DRAM controller 18a.

PAGE 19/22 * RCVD AT 3/29/2004 4:37:57 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:9253718187 * DURATION (mm-ss):05-38

Thus, even if Chauvel were combined with Petersen, the resulting structure would not teach or suggest Applicant's Claim 1.

In addition, there is no motivation to combine Petersen and Chauvel, absent the Applicant's own specification.

The Examiner indicates that the combination of Petersen and Chauvel is proper because the traffic controller 18 of Chauvel would "associate an initial priority value for a plurality of memory access requests". However, prioritizing memory access requests has nothing to do with the data alignment operations suggested by Petersen.

For these reasons, Claim 1 is allowable over Petersen in view of Chauvel. Claims 2-14, which depend from Claim 1, are allowable over Petersen in view of Chauvel for at least the same reasons as Claim 1.

In addition, Claim 3 recites "the memory read aligner is configured to provide data words that are fully aligned with the system bus during fly-by write operations", and Claim 4 recites "the peripheral read aligner is configured to provide data words that are fully aligned with the system bus during fly-by read operations."

As described above, Petersen fails to teach data words that are fully aligned with the host bus. For example, Table 1 of Petersen explicitly illustrates that non-aligned data words are transferred on the host bus during write many of the write cycles. Chauvel does not remedy this deficiency of Petersen, as prioritizing memory access requests would not change the content of the memory accesses.

For this additional reason, Claims 3 and 4 are allowable over Petersen in view of Chauvel.

PAGE 20/22 * RCVD AT 3/29/2004 4:37:57 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:9253718187 * DURATION (mm-ss):05-38

SN: 09/888,321

Claims 31 and 36 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Petersen in view of Yarch et al. (U.S. Patent No. 5,761,532), hereinafter "Yarch".

Claim 31, which depends from Claim 24, is allowable over Petersen for at least the same reasons as Claim 24. Yarch fails to remedy the above-described deficiencies of Petersen. Consequently, Claim 31 is allowable over Petersen in view of Yarch.

Claim 36, which depends from Claim 33, is allowable over Petersen for at least the same reasons as Claim 33. Yarch fails to remedy the above-described deficiencies of Petersen. Consequently, Claim 36 is allowable over Petersen in view of Yarch.

Claims 17-22 have been objected to for being dependent upon a rejected base claim. The Examiner has indicated that these Claims would be allowable if rewritten in independent form, including all the limitations of the base claim and any intervening claims. However, because Applicant believes that the base Claim 15 is allowable for reasons cited above, Applicant is not amending Claims 17-22 at this time.

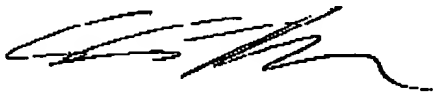
PAGE 21/22 * RCVD AT 3/29/2004 4:37:57 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:9253718187 * DURATION (mm-ss):05-38

SN: 09/888,321

CONCLUSION

Claims 1-36 are pending in the present Application. Reconsideration and allowance of these claims is respectfully requested. If the Examiner has any questions or comments, he is invited to call the undersigned.

Respectfully submitted,



E. Eric Hoffman
Reg. No. 38,186
Attorney for Applicant
BEVER, HOFFMAN & HARMS, LLP

Customer No.: 022888
Tel. No.: (925) 895-3545
Fax No.: (925) 371-8187

CERTIFICATE OF TRANSMISSION (37 C.F.R. 1.8(a))

I hereby certify that, on the date shown below, this correspondence is being transmitted by facsimile to the Patent and Trademark Office.

Date: 3-29-04 Signature: Carrie Peddicke

PAGE 22/22 * RCVD AT 3/29/2004 4:37:57 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:9253718187 * DURATION (mm-ss):05-38